REMARKS

The present application is drawn to claims 16-19 and new claims 21-28, which depend therefrom. Claims 16-18 were rejected. Claims 19 and 21-28 were indicated allowable if rewritten in independent form.

Claim Rejections

Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. patent No. 5,625,591 to Kato et al. ("Kato") in view of U.S. patent No. 6,275,961 to Roohparvar ("Roohparvar"). This rejection is respectfully traversed.

Claims 16-18 are directed to a method of margin testing a single polysilicon ("single poly") EEPROM cell that involves evaluating an erase margin voltage in the single polysilicon EEPROM cell, including sweeping a voltage applied to the control gate of the EEPROM cell through a range of voltages above about 0 V.

The Examiner relies upon Kato for a description of the structure and operation of an EEPROM cell. However, the EEPROM cell described in Kato has a "control gate 12 of a second poly silicon layer [] formed on the floating gate 11 via an insulating film 19" (Kato, column 1, lines 35-37). As noted in the present application in the paragraph bridging pages 1 and 2,

> EEPROM cells may have a variety of configurations. In particular, EEPROMs may be formed from single or double polysilicon processes. A double polysilicon process EEPROM has a polysilicon control gate capacitively coupled to its floating gate. A single polysilicon process EEPROM does not have a polysilicon control gate, but instead has a second heavily doped diffusion implant in the cell's substrate which is capacitively coupled to its floating gate. Margin testing of single polysilicon ("single poly") EEPROMs are the focus of this invention.

Thus, Kato relates to a double polysilicon ("double poly") EEPROM cell, and not a single poly EEPROM cell as claimed. As noted in the background section of the present application, particularly at page 6, for example, margin testing of single poly EEPROMs is more problematic than margin testing of double poly EEPROMs due to the backward biasing in single poly EEPROM substrates.

The Examiner relies upon Roohparvar for a description of sweeping voltages in the context of a non-volatile memory cell (e.g., an EEPROM cell). Roohparvar describes sweeping voltages to determine I and V characteristics of an array of memory cells. However, single poly EEPROM cells are not specifically addressed. Further, according to the Roohparvar method, voltages are swept across the source and drain lines rather than the control gate, as recited in the

claims in issue. Accordingly, Roohparvar does not remedy the deficiency of Kato with regard to the single poly EEPROM aspect of the claimed invention, and also does not teach the sweeping of voltages across the control gate of a single EEPROM cell.

Accordingly, the EEPROM devices and operations described by Kato and Roohparvar do not relate to the issues addressed, nor the structures or methods described and claimed in the present application. Claim 16 has been amended for purposes of clarity by repeating the recitation of the single polysilicon EEPROM in the preamble in the body of the claim. The intent of this amendment is not to modify the scope of the claim, but rather to more clearly define that which is claimed. Since, as explained above, the cited art does not teach or suggest margin testing of a single polysilicon EEPROM cell in accordance with the present invention, claims 16-18 are respectfully submitted to be patentable over the cited art, and withdrawal of the rejection under section 103 is respectfully requested.

Claim 19 has been indicated allowable if rewritten in independent form. The claim has been amended to recite an indefinite rather than a definite article for the term "drain line" to comply with antecedent basis requirements, correcting a clerical error. For at least the reasons noted above with regard to claim 16-18, claim 19 is believed to be allowable in its current dependent form.

Allowable Subject Matter

Claims 19 and 21-28 were indicated allowable if rewritten in independent form. This indication of allowability is gratefully acknowledged.

As noted above, claim 16 and the remaining claims, which depend from claims 16 directly or indirectly, are believed to be allowable substantially as filed. However, in order to simplify the remaining issues for further prosecution, claims and 21 and 24, from which claims 22-23 and 25-28 depend, respectively, have been rewritten in independent form. The scope of these claims is unchanged by these amendments, and it should be understood that these amendments are made solely to simplify and expedite prosecution. Accordingly, an indication of allowance is respectfully requested for claims 21-28.

The allowability of claim 19 in its dependent form is argued above.

Conclusion

Applicants believe that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be

reached at the telephone number set out below. If any fees are due in connection with the filing of this paper, the Commissioner is authorized to charge such fees to Deposit Account 500388 (Order No. ALTRP022D2).

Respectfully submitted,
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